Novel In-Situ Fabricated Josephson Junctions: Trilayer on a Substrate Slope

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***Abstract*—We demonstrate a high-temperature superconductor (HTS) Josephson junction geometry using only *in situ* interfaces and with the current flowing in the a–b plane of the HTS. The trilayer on a substrate slope (TOSS) junction is a HTS-barrier-HTS structure deposited *in situ* on top of a pre-etched slope in the substrate. We present initial results on the fabrication and testing of $YBa_2Cu_3O_{7-\delta}$ TOSS junctions with a Ga-doped $PrBa_2Cu_3O_{7-\delta}$ barrier. These devices display resistively shunted junction like I–V characteristics with characteristic voltages up to 5 mV at 4.2 K. The TOSS junction concept is of interest for fundamental studies of interfaces in HTS and can also be applied to an integrated circuit technology.**

I. Introduction

THE realization of integrated high critical temperature (high-T_c) Josephson junction circuits is still an uncompleted task [1]. A lot of effort has been invested in creating a technology using ramp-edge-type junctions [2]–[5] which offer several advantages over other types of high-T_c device. The ramp-type geometry allows a small area contact in the a–b plane which in turn lowers the demands on the barrier: Josephson transport in the a–b plane can be achieved using a relatively thick barrier compared to c-axis junctions and their characteristics can be tuned by varying the barrier material and thickness. Despite these benefits all ramp-type technologies developed so far suffer from low reproducibility. However progress is fast and it should be noted that recently developed interface-engineered junctions [4] brought the 1-sigma spread down to 7.9% for 100 junctions [5].

It is well known that one reason for low reproducibility in HTS junctions are the exceptional interfacial difficulties of the HTS materials. Even a very short exposure to air during fabrication has been shown to significantly degrade ramp-junction performance and increase the spread of parameters [6]. A significant step in formation of *in-situ* electrode/barrier interface in $YBa_2Cu_3O_{7-\delta}$ (YBCO)/Au/Nb junctions has recently been taken by H-J H Smilde and co-workers [7]. They report on increased transparency of the interface by the *in-situ* deposition of a thin YBCO layer on the ramp edge before the deposition of the Au barrier. Another way to circumvent the problem is to make junctions completely *in situ*. This has been reported by many groups using planar a- or c-axis oriented trilayer junctions with different kinds of barriers [8]–[12]. Trilayer junctions made from a-axis oriented films [8]–[10] are hard to integrate because of the anisotropy in the current transport. C-axis junctions [11], [12], due to the extremely short coherence length in the c-direction (<2 nm), have to be made using extremely thin and uniform barriers—a challenging task for the current thin film growth technologies.

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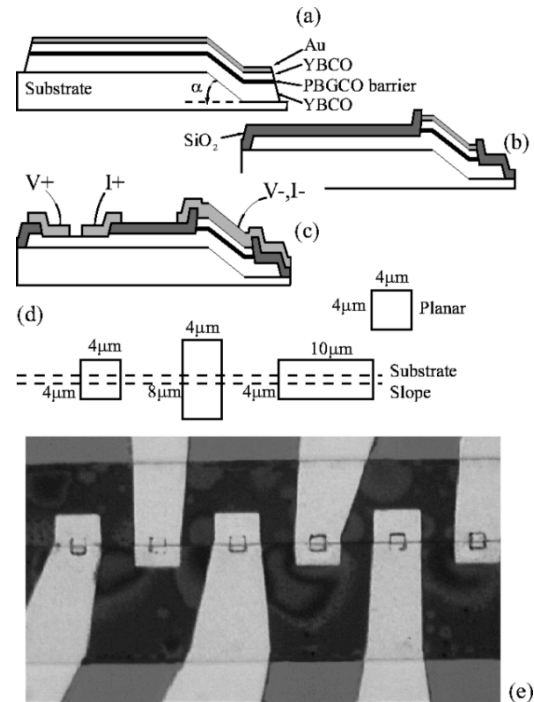

Fig. 1. (a) A YBCO(striped)-PBGCO(black) trilayer capped with a thin *in-situ* gold layer (light gray) has been deposited on an etched substrate slope with angle α. (b) The junction mesas are etched and the SiO_2 insulator (darker gray) is defined by lift-off trough the same photoresist mask. (c) Vias are etched trough the insulator and gold contacts are added. (d) Schematics showing some of the different type of junctions examined: TOSS junctions with different widths *along* and *across* the slope, and planar junctions where no a–b plane transport is to be expected. (e) Micrograph showing 6 4×4 μm TOSS junctions. The darker region is the YBCO bottom electrode and the horizontal middle line is the substrate slope.

In this letter we introduce a junction geometry that allows both a–b plane current transport and *in situ* barrier formation.

II. Fabrication

The principles of the fabrication of a Trilayer On a Substrate Slope (TOSS) junction are shown in Fig. 1. First a slope of about 15° and 300 nm deep is etched in an $SrTiO_3$ (STO) substrate using 250 V Ar-ion milling. The resist mask is formed using proximity exposure [13] followed by a postexposure bake at 120°C. The angle of incidence of the Ar-ions was 45° and the

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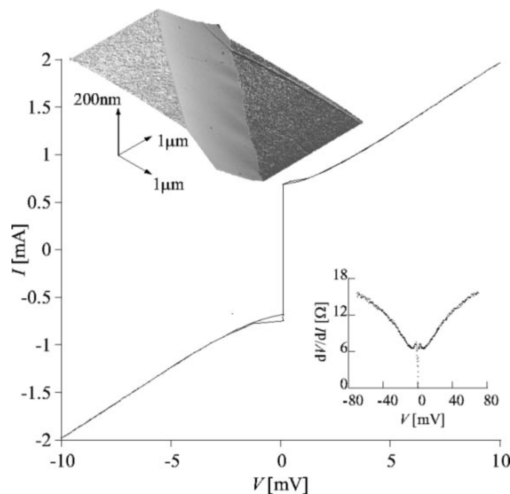

Fig. 2. Typical I–V and dV/dI–V curves for a 4×4 μm, 25 nm barrier, TOSS junction at 4.2 K. The upper inset show an atomic force microscope image of a substrate slope after annealing at 760°C in 0.6 mbar oxygen.

substrate was rotated during etching. Using the above described technique we can produce slopes with any desirable angle facing in any direction so that the placement of junctions and wiring is not restricted in any way.

Etched substrates were examined in AFM both before and after a high temperature anneal at the same temperature and oxygen pressure used for the deposition of YBCO. The surface of the etched STO slopes was found to be smooth (~0.5 nm peak-to-valley roughness) in both cases. The substrates were even smoother after the high temperature anneal in contrast to the case of etched YBCO ramps, see inset of Fig. 2.

The etched substrates were mounted in a pulsed laser deposition (PLD) chamber where a trilayer of YBCO—$PrBa_2Ga_{0.4}Cu_{2.6}O_{7-\delta}$ (PBGCO) -YBCO was grown followed by the deposition of a thin *in situ* gold layer. The nominal thickness of the bottom and top YBCO layers was 150 and 100 nm respectively. The PBGCO barrier thickness was varied between 15 and 25 nm in different samples. The trilayer was subsequently patterned to define the bottom YBCO electrode, Fig. 1(a). To etch the junction area and define the corresponding insulator vias we use a self-aligned technology with a resist mask (S-1813) on top of a liftoff layer (Shipley LOL-2000). The same S-1813/LOL mask is then used to pattern the SiO_2 insulator by liftoff directly after etching the junction mesas, without any further photolithography, Fig. 1(b). Subsequently a via hole is etched through the SiO_2 to the bottom YBCO and gold contacts are deposited, Fig. 1(c). To facilitate the alignment of the contacts during lithography we only patterned one gold lead to each junction so the junction characteristics are obtained using three point measurements. The contact resistance varied between 1–3 Ω and has been subtracted from all the data presented in this letter. A micrograph showing six TOSS junctions from one of the samples is presented in Fig. 1(e).

III. Experimental Results

Three samples were produced in total with 35 test structures of different types on each sample. In all samples the gold adhesion to the SiO_2 layer was very weak, this made bonding extremely difficult so we were not able to measure all the junctions on all the samples. The nominal barrier thickness was 15, 20, and 25 nm in the three samples, however, due to bonding problems the only sample that could be thoroughly measured was the one with 25nm barrier thickness. The measurable junctions on samples with 15 nm and 20 nm thick barrier showed very large critical currents, up to 4 respectively 3 mA for a 4×4 μm TOSS junction, with flux flow like I–V curves probably due to heating effects in the small counter electrode at high bias currents. However, planar trilayer junctions on the same samples showed almost linear resistivity in the $k\Omega$ range suggesting that the transport in the TOSS junctions is dominated by a–b plane coupling and that the barrier is free from shorts (at least free from shorts in the planar part). The sample with 25 nm nominal barrier thickness showed the most RSJ-like I–V curves, see Fig. 2. Curves of this type were observed in all 30 junctions measured on this sample. This sample also had planar c-axis junctions, 4×4 and 4×8 μm large both on the etched and unetched part of the substrate. As in the case of the other samples these junctions showed resistive behavior.

Most of the junctions were 4 μm long across the substrate slope and 4–10 μm wide along the slope, see Fig. 1(d). We also fabricated junctions that were 8 μm long across the substrate slope and 4 μm wide along the slope. These junctions showed a critical current, I_c, comparable to the 4×4 μm junctions, once again indicating that the TOSS junctions are dominated by a–b plane coupling in the small area that lies on the substrate slope. In general the I_c of the junctions scales with the width of the junction along the ramp but we cannot rule out that the size of the planar part of the junction migth also play an important role. The intrinsic shielding of the junctions—small mesas on a large YBCO plane, makes it difficult to modulate the junctions with magnetic field directed normal to the substrate. The maximum suppression of the I_c we could obtain by a magnetic field normal to the substrate was about 25% however, our experimental setup is limited to quite small magnetic fields. We believe that a stronger magnetic field directed in the plane of the barrier will give a more accurate estimation of the amount of excess current. A set-up allowing stronger magnetic fields, both parallel and perpendicular to the substrate is being developed. The ac-Josephson effect has been observed in the junctions; see the inset of Fig. 3.

Judging from the results mentioned above, the current is mainly transported in the a–b plane where the cross sectional area is about $1.2 \cdot 10^{-8}$ cm^2 for a 4 μm wide junction. Typically these junctions have critical currents around 0.6 mA for the 25 nm barrier junctions at 4.2 K (see the inset of Fig. 4) and the critical current density, J_c, is about $6 \cdot 10^4$ A/cm^2 which is quite a large value compared to reported results on ramp-type junctions with similar barrier thickness [1], [3]. This is an indication of the high transparency of the *in situ* formed interface between the barrier and the electrodes. The result suggests that it might be possible to fabricate TOSS junctions with thicker barriers than devices with *ex situ* formed barrier and thus improving junction uniformity.

The temperature dependence of the junction parameters is presented in Figs. 3 and 4. The critical temperature is around 84 K for most of the junctions and does not vary with I_c. The

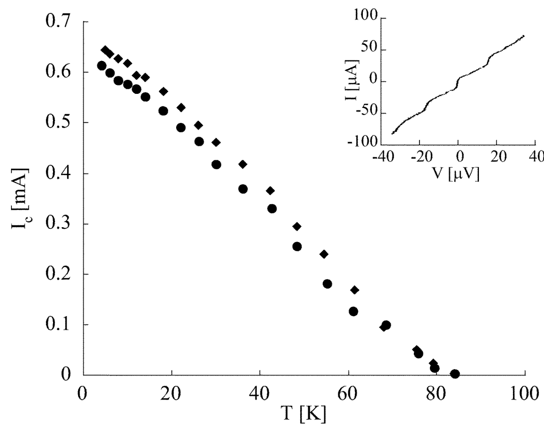

Fig. 3. Dependence of the critical current, I_c, on temperature for two different TOSS junctions. The filled circles curve are taken from a junction 8 μm wide *across* the slope and 4 μm wide *along* the slope, the diamond curve corresponds to a 4×4 μm TOSS junction. The inset shows an example of an I–V curve of a TOSS junction irradiated with 4 GHz microwaves. At this particular microwave power the odd steps are almost completely suppressed. All curves are taken from the 25 nm barrier sample.

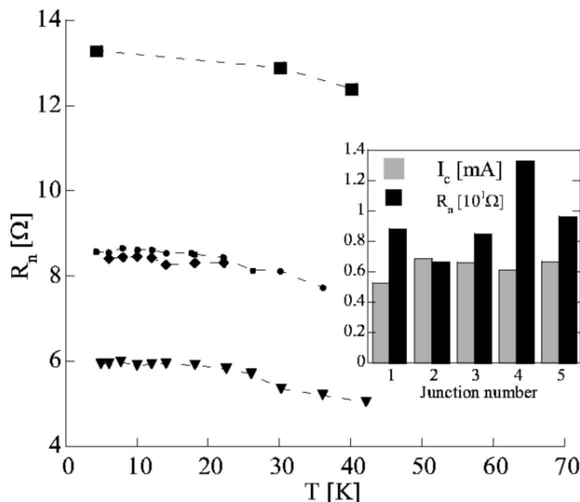

Fig. 4. The temperature dependence of the normal state resistance taken at around 5 mV for four different TOSS junctions. The filled circles and diamonds corresponds to the same junctions as in Fig. 3. The inset shows the $I_c s$ and $R_n s$ at 4.2 K for a set of typical 4×4 μm TOSS junctions. The barrier thickness is 25 nm in all cases.

values of the normal state resistance, R_n, varies in general with the applied voltage, see the inset of Fig. 2. In Fig. 4 the R_n values are measured at 5 mV, the resistance above 20 mV is in general twice as high.

Uniformity between junctions is one of the most crucial factors for multi-junction circuitry. Most of the 4×4 μm TOSS junctions had $I_c s$ of around 0.6 mA and $R_n s$ of around 8 Ω at 5 mV (see the inset of Fig. 4). This gives a value of the $I_c R_n$ product of approximately 4.5 mV. However, since the exact amount of excess current has not been properly examined the fundamental $I_c R_n$ product might be lower. On the other hand, the nearly complete suppression of the critical current under microwave irradiation (see inset of Fig. 3) suggests that the amount of excess current is low.

Since the tested junctions are of significantly different geometries it is difficult to quantitatively compare them and determine the spread before the exact transport properties are established. When comparing junctions of the same geometry the TOSS are uniform both in I_c and R_n. This is relatively surprising, keeping in mind that these results are based on the very first batch of 3 samples: No optimization of film quality, substrate etching, barrier composition and thickness has yet been performed. We are encouraged by the fact that the PBGCO barrier probably can be thicker without reaching too low J_c values. Perhaps even more promising is the possibility of using a highly resistive barrier or an interface engineered barrier.

IV. Conclusion

We have demonstrated a trilayer Josephson junction technology for HTS in which junctions with the current transport in the *a–b* plane are fabricated completely *in situ*. The junctions are reproducible and easy to fabricate. More thorough experiments are needed in order to determine the spread and the exact transport properties of TOSS junctions.

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