

## Submicron $\text{YBa}_2\text{Cu}_3\text{O}_x$ ramp Josephson junctions

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Submicron  $\text{YBa}_2\text{Cu}_3\text{O}_x/\text{PrBa}_2\text{Cu}_{2.6}\text{Ga}_{0.4}\text{O}_x/\text{YBa}_2\text{Cu}_3\text{O}_x$  ramp-type Josephson junctions were fabricated and tested. The submicron bridges in the top electrode were patterned by  $e$ -beam lithography and Ar ion milling through an amorphous carbon ( $a$ -C) mask. Junctions with width ranging from 0.2 to 8  $\mu\text{m}$  and oriented along different crystal directions of  $\text{YBa}_2\text{Cu}_3\text{O}_x$  have been produced. Current–voltage characteristics show a behavior consistent with the resistively shunted junction model with small excess current. Junction critical current densities of about 10  $\text{kA}/\text{cm}^2$  and characteristic voltages up to 6 mV were measured at 4.2 K for the submicron junctions. Junctions along different crystal orientations showed different characteristics suggesting an influence from the  $d$ -wave order parameter. © 2002 American Institute of Physics. [DOI: 10.1063/1.1448176]

As the scale of the semiconductor world goes into the submicron range, similar moves are likely in superconductor electronics. Smaller Josephson junctions with a high density of the superconducting critical current  $J_c$  permit, for example, rapid single flux quantum (RSFQ) circuits with higher integration and higher speeds. Ramp-type Josephson junctions based on high-temperature superconductors, namely  $\text{YBa}_2\text{Cu}_3\text{O}_x$  (YBCO), satisfy these conditions having high  $I_c R_N$  product (up to 8 mV at 4.2 K) making possible THz frequencies of RSFQ circuits ( $I_c$  is the critical current of the Josephson junction and  $R_N$  is the junction resistance in the normal state).<sup>1</sup>

The fabrication of micrometer size ramp Josephson junctions has been reported by several groups so far.<sup>1–4</sup> Moreover, simple RSFQ circuits in ramp junction technology have been reported recently.<sup>5</sup> In order to investigate the possibility of a submicron ramp junction technology for high temperature superconductor circuits we produced and studied ramp junctions with submicron widths. Furthermore, we implemented a layout that allowed us to test the impact of the  $d$ -wave superconducting order parameter in YBCO on junction characteristics.<sup>6</sup>

A 150 nm thick layer of YBCO covered by 150 nm insulator of  $\text{PrBa}_2\text{Cu}_3\text{O}_x/\text{SrTiO}_3/\text{PrBa}_2\text{Cu}_3\text{O}_x$  was deposited on a  $\text{SrTiO}_3$  substrate using pulsed laser deposition. The bottom electrode was defined using photolithography with a standard Shipley S1813 photoresist. After development of the resist pattern the sample was postbaked in air at 120 °C for 30 min in order to obtain a photoresist mask with a rounded edge profile [Fig. 1(a)]. The bottom electrode and insulator multilayer structure were etched by an argon ion beam with an energy of 250 eV and a current density of 0.2  $\text{mA}/\text{cm}^2$ . During etching the sample was tilted at 45° and rotated to achieve a smooth, low angle ramp in the bottom electrode. The photoresist mask was removed in oxygen and argon plasma. A last cleaning of the ramps was made using a

low energy 100 eV argon ion-beam etching at 0.1  $\text{mA}/\text{cm}^2$  for 30 min. The sample was then immediately transferred into the deposition chamber, annealed at 0.2 mbar oxygen atmosphere for 30 min, and then the  $\text{PrBa}_2\text{Ga}_{0.4}\text{Cu}_{2.6}\text{O}_x$  (PBGCO) barrier and YBCO top electrode were subsequently deposited [Fig. 1(b)]. The thickness of the top electrode was always 150 nm, while that of the barrier was reduced from 25 to 13 nm as our technology progressed. The presented data are from samples with a 13 nm barrier. A 30 nm thick protective gold layer was deposited on the top electrode. Via holes to the bottom electrode were opened by photolithography and argon ion-beam etching [Fig. 1(c)]. Another gold layer was deposited by  $e$ -beam evaporation and patterned to define bonding contact pads and alignment marks for the  $e$ -beam lithography [Fig. 1(d)]. Before  $e$ -beam lithography the chip was covered with a 100 nm thick amorphous carbon,  $a$ -C, layer to provide a hard etching mask and a thin 30 nm gold layer underneath the carbon to prevent charge-up during the exposure. Both layers were deposited by electron beam evaporation.

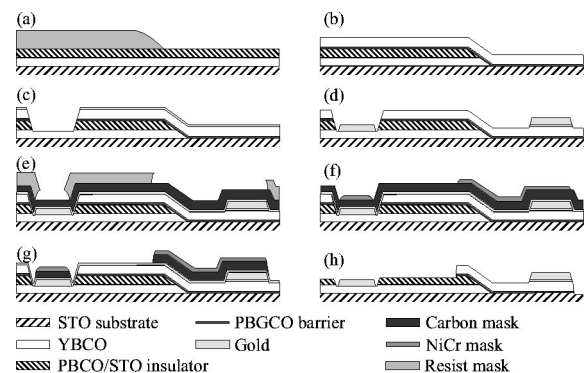


FIG. 1. A schematic of the fabrication process: (a) bottom electrode with insulator covered by a photoresist mask; (b) deposition of the PBGCO barrier and YBCO top electrode; (c) deposition of the protective gold layer and opening of the via holes to the bottom electrode; (d) gold contact pads and alignment marks for  $e$ -beam lithography; (e) the gold and carbon layers, covered by the developed  $e$ -beam resist; (f) the NiCr layer deposited through the  $e$ -beam resist lift-off mask; (g) the NiCr mask transferred to the carbon layer by oxygen plasma etching; and (h) a cross section of the sample.

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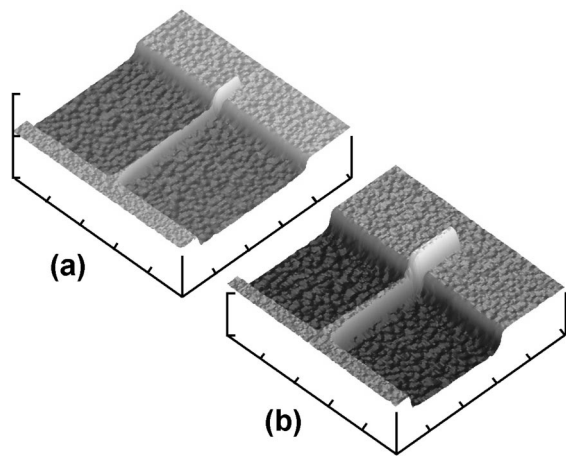


FIG. 2. The AFM images of: (a) 0.2  $\mu\text{m}$  and (b) 0.5  $\mu\text{m}$  junction. The horizontal scale is 2  $\mu\text{m}/\text{div}$ . The vertical scale is (a) 900  $\text{nm}/\text{div}$  and (b) 600  $\text{nm}/\text{div}$ . The measured widths correspond to the nominal designed widths.

A double-layer resist consisting of 10% Nano-Copolymer and 2% poly(methyl methacrylate) was used for the  $e$ -beam lithography. After development of the resist [Fig. 1(e)], the pattern was transferred to a layer of  $e$ -beam-evaporated NiCr using a standard lift-off technique [Fig. 1(f)]. By etching the carbon in a 50 W oxygen plasma through the patterned NiCr layer we obtained a hard  $a$ -C mask [Fig. 1(g)]. The junctions were finally formed by argon ion milling at 0.1  $\text{mA}/\text{cm}^2$  and 250 eV through the  $a$ -C mask. After stripping of the residual carbon in a low-power oxygen plasma the thin gold layer was finally removed by argon ion-beam etching [Fig. 1(h)].

Six samples were produced and tested with 23 junctions on each sample with widths ranging from 0.2 to 8  $\mu\text{m}$ . Slightly different processing parameters were used for the different samples as our technology progressed. To test the limit of the technology, 0.2  $\mu\text{m}$  wide junctions were fabricated on the first samples. The multilayer structures and junctions were examined by an atomic force microscope (AFM) that revealed smooth film surfaces and ramps with angles around  $30^\circ$  and junction widths corresponding to the nominal widths defined in the mask (Fig. 2). The Josephson effect was observed in junctions of all widths, even for the 0.2  $\mu\text{m}$  wide junctions. However, the critical current density  $J_c$  in these junctions was systematically measured to be ten times lower than the one measured for the wider junctions. This motivated us to restrict our further studies on junctions with widths equal to or larger than 0.5  $\mu\text{m}$ .

To test junctions with current transport along different crystal directions, samples were designed with the bottom electrode as an octahedron and the top electrode providing current flow perpendicular to the sides of the octahedron [Fig 3(a)]. (Similar layouts were implemented to study transport in YBCO-Ag junctions<sup>7</sup> and underdoped YBCO junctions.<sup>8</sup>) Assuming that  $d_{x^2-y^2}$  pairing symmetry is predominant in YBCO two different types of junctions are realized in our samples depending on the orientation of the ramp edge with respect to the  $a$ - $b$  crystal axes of YBCO. We denote the type of junctions, where the ramp edge is  $\pi/4$  misaligned from  $a$ - $b$  crystal axes of YBCO, as  $\pi/4$ - $\pi/4$  junctions, and as 0-0 junctions in the case where the edge is parallel (perpendicular) to the axes [Figs. 3(b) and 3(c)].

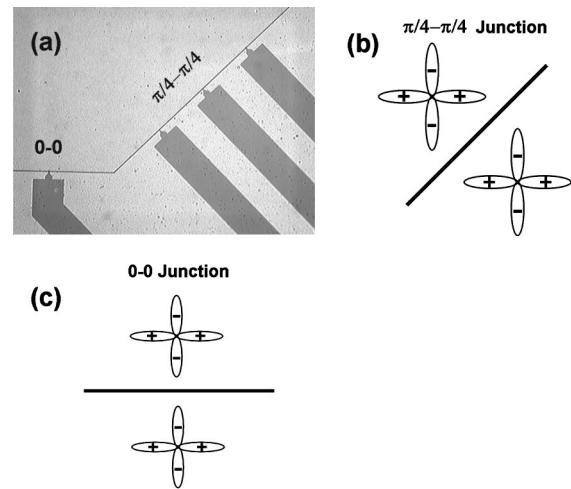


FIG. 3. (a) A micrograph of one of the fabricated samples showing a corner of the octahedron with 0-0 and  $\pi/4$ - $\pi/4$  junctions. Schematic of the mutual orientation of the ramp edge and the superconducting order parameter in YBCO electrodes for (b)  $\pi/4$ - $\pi/4$  and (c) 0-0 junctions.

The tested junctions of the 0-0 type have current-voltage ( $I$ - $V$ ) curves that can be described with a model of a resistively shunted junction (RSJ) with  $J_c \sim 10^4 \text{ A}/\text{cm}^2$ ,  $I_c R_N \sim 1$ -6 mV, and  $R_N A \sim 10^{-7} \Omega \text{ cm}^2$  ( $A$  is the junction area) [Fig. 4(a)].<sup>9</sup> These levels of  $J_c$  and  $R_N A$  for the 0-0 junctions agrees with the measurements by Verhoeven *et al.*<sup>1</sup> [The agreement is good provided a factor of  $\tan(30^\circ)/\tan(20^\circ)$  is taken into account since the measurements in Ref. 1 are from ramp junctions with  $20^\circ$  ramps and

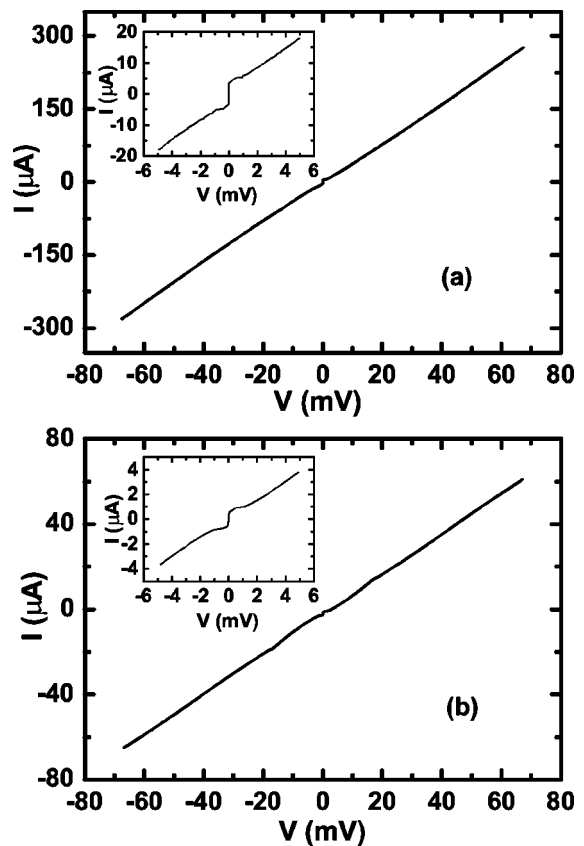


FIG. 4.  $I$ - $V$  curves for two 0.5  $\mu\text{m}$  wide ramp junctions with 13 nm thick PBGCO barrier of (a) 0-0 and (b)  $\pi/4$ - $\pi/4$  types. The low voltage parts of the  $I$ - $V$  curves ( $V < 5 \text{ mV}$ ) are shown in the corresponding insets.

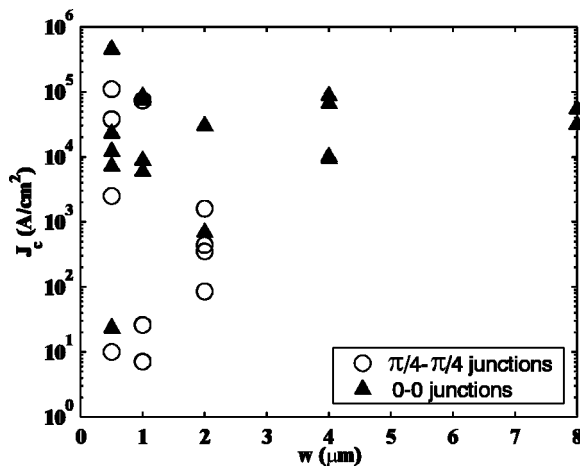


FIG. 5. Dependence of the critical current density on the junction width. Data for junctions of 0–0 and  $\pi/4-\pi/4$  types from two different samples are shown.

the barrier thickness is measured normal to the substrate surface.] An excess current has been observed for 0–0 junctions with widths larger than the estimated doubled Josephson penetration depth at 4.2 K. Figure 5 presents the  $J_c$  of the junctions in two of the fabricated samples with a barrier thickness of 13 nm, as a function of the junction width. It can be seen from Fig. 5, that the  $J_c$  values scale with the width of the junction for the majority of the tested 0–0 junctions suggesting homogeneity of the PBGCO barrier.

Statistics are not enough to analyze the spread of  $J_c$  for the  $\pi/4-\pi/4$  junctions, but the values of  $J_c$  for the  $\pi/4-\pi/4$  junctions are in general 1 or 2 orders of magnitude lower than that of the 0–0 ones. We can attribute that neither to the difference in the slope and roughness of the ramp surface nor to the difference in barrier transparency. The latter one is of the same order of magnitude both for 0–0 and for  $\pi/4-\pi/4$  junctions, and our AFM measurements revealed similar undulation and roughness of the ramp edges regardless of ramp orientation. One possible explanation of the effect comes from the mutual orientations of YBCO electrodes to the ramp edge, namely the coincidence of the direction of the current with the node in the  $d$ -wave superconducting order parameter in YBCO. However, relatively large values of the  $J_c$  has been predicted for  $\pi/4-\pi/4$  type junctions,<sup>10</sup> in contradiction to our results.

No zero bias conductance peaks (ZBCPs) associated with the formation of the midgap states on the node surfaces of the  $d$ -wave superconductors have been observed for 0–0 and  $\pi/4-\pi/4$  junctions.<sup>11</sup> In the case of  $\pi/4-\pi/4$  junctions the absence of the ZBCP may indicate well-defined midgap states with little or no broadening.<sup>10</sup>

In conclusion, a technology for fabrication of submicron ramp Josephson junctions with PBGCO barriers has been developed. Junctions of two different types have been fabricated and tested: 0–0 junctions with the ramp edge parallel or perpendicular to the  $a-b$  crystal axes of YBCO and  $\pi/4-\pi/4$  junctions with the ramp edge making an angle of  $\pi/4$  with respect to the axes. The 0–0 junctions show RSJ behavior with the  $I_c R_N$  products around 1–2 mV and critical current densities on the order of  $10^4$  A/cm<sup>2</sup> at 4.2 K. Small values of  $J_c$  have been observed in  $\pi/4-\pi/4$  junctions, probably due to a node-to-node orientation of the  $d$ -wave order parameter of YBCO electrodes. The obtained results indicate that  $\pi/4-\pi/4$ -type junctions are not suitable for the design of superconducting integrated circuits.

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